AY-5-8100 AY-5-8102

Radio Receiver Frequency Counter / Display Drivers

FEATURES

- Three frequency ranges: MW 2999kHz, SW 29.995MHz, VHF 299.95MHz
- IF offset: 460kHz (AY-5-8100) or 455kHz (AY-5-8102) on MW and SW, 10.7MHz on VHF
- Channel mode 0-99 channel spacing 300kHz. Standard part channel 0 is 87MHz
- High voltage segment and digit outputs give direct drive of fluorescent displays.
- Inversion control for segment outputs.
- Direct drive of liquid crystal displays.
- 1.28MHz master clock input frequency.
- 300kHz input with 8ms sample time.
- TTL compatible inputs and outputs.
- 50Hz output to drive the AY-5-1200A digital clock.

DESCRIPTION

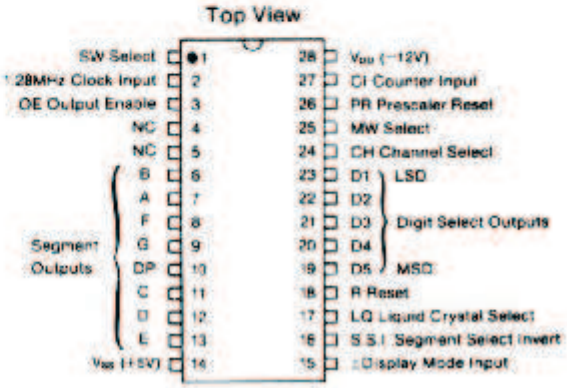
The AY-5-8100/8102 are 4½ digit frequency counters for use in Radio Receivers. Three main frequency ranges are provided. 2999kHz and 29.995MHz (with a 460kHz IF offset on the AY-5-8100 and a 455kHz IF offset on the AY-5-8102) and 299.95MHz with a 10.7MHz IF offset. For use in VHF FM receivers a channel mode is available. In this mode a channel number from 0 to 99 is displayed together with a "+" or "−" sign for tuning indication. In this mode the IF is 10.7MHz and channel 0 is 87MHz.

The outputs are multiplexed in five time slots onto a seven segment bus. Digit and segment outputs have high voltage capability and will drive fluorescent displays directly. A pin option allows the driving of liquid crystal displays using the two-frequency multiplexing system.

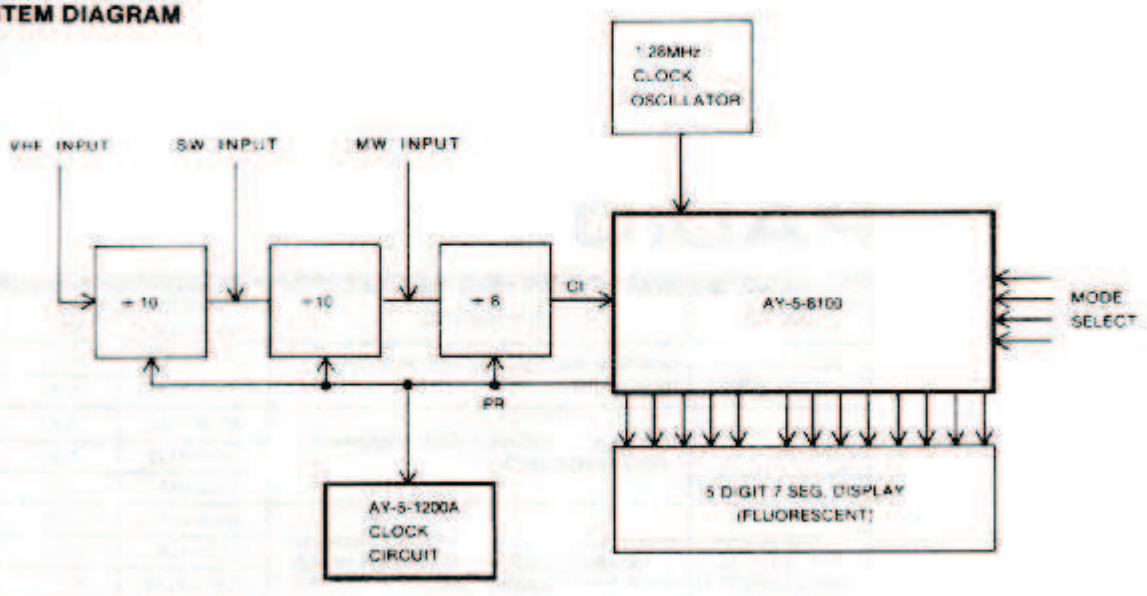
PIN CONFIGURATION

28 LEAD DUAL IN LINE

Top View



SYSTEM DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	SW Select	Selects 29.995MHz counter range when at logic '0'. See Mode Select truth table.
2	1.28MHz Clock	Master clock input controls timing of whole system.
3	Output Enable	Disables the outputs when taken to logic '0'.
4	N.C.	
5	N.C.	
6-13	Segment Outputs	The digits to be displayed are output on these pins in 7 segment code. They are at logic '1' to display. These outputs will also drive fluorescent, liquid crystal and low current LED displays.
14	V_{SS}	Positive supply.
15	±Display Mode Input	Selects either combined or separate + or − display when in channel mode. Logic '0' selects combined mode. In the combined mode the horizontal bar is output on segment "g" and the vertical bar on segment "f". In the separate mode the − sign is output on segment "g" and the + sign on segment "f".
16	Segment Select Invert	When taken to logic '1' inverts the Segment Select outputs (Note 1).
17	Liquid Crystal Select	When taken to logic '1' the output timing is arranged to drive liquid crystal displays using two frequency multiplexing.
18	Reset	Master reset to all counters and registers. Resets when at logic '1'.
19-23	Digit Select Outputs D1-D5	These outputs sequentially select the digit to be displayed. They are normally at logic '1' to display. The outputs are high voltage and are capable of driving fluorescent and liquid crystal displays directly. Each digit is on for 4ms. A bonding option gives inverted outputs.
24	Channel Select	Selects channel mode when at logic '0' and SW and MW are at logic '1'. See Mode Select truth table.
25	MW Select	Selects 2999kHz counter range when at logic '0'. See Mode Select truth table.
26	Prescaler Reset	This output resets the external prescaler divider at logic '0' during count interval.
27	Counter Input	Frequency measuring input. Frequency range 10kHz to 600kHz.
28	V_{DD}	Negative supply.

NOTE:
1. If the digit invert bonding option is used (bonding to logic '1') the SSI input logic sense will be inverted.

FREQUENCY COUNTER OPERATION

The frequency counter section is intended to work with an external prescaler. The three frequency ranges require division ratios of 8, 80 and 800. The appropriate IF offset is loaded into the counter before measuring. The local oscillator must always be at a higher frequency than the receiver frequency.

Measurement period	8m
Reading rate	50 per second
Master clock frequency	1.28MHz

Mode	Display Range D5	D4	D3	D2	D1		Discrimination	Prescaler	IF
MW	2	9	9	9		kHz	1kHz	÷ 8	460
SW	2	9 •	9	9	5	MHz	5kHz	÷ 80	460
FM	2	9	9 •	9	5	MHz	50kHz	÷800	10.7
CH	÷	9	9				300kHz	÷ 600	10.7
COUNT	2	9	9	9	5		0.5kHz	÷ 8	10

NOTES:
1. Leading zeros are blanked.
2. In Channel Mode the + or − signs are lit if the receiver is more than 50 kHz off tune.
3. The IF offset is mask programmed and can in principle be made to any value.
4. In Channel Mode, Channel 0 = 87 MHz.

MODE SELECTION

MW	SW	CH	OE	Mode
0	1	X	1	MW
1	0	X	1	SW
1	1	1	1	VHF
1	1	0	1	VHF/Channel
0	0	0	1	Counter mode
X	X	X	0	Clock

DISPLAY OUTPUT

The output is in 7 segment form multiplexed into five time slots at a rate of 50Hz. All the display outputs have high voltage capability and will drive fluorescent displays directly. LED displays can either be driven directly or with simple interfacing depending on the digit size.

A pin selected option allows the direct driving of liquid crystal displays using two frequency multiplexing (125Hz and 8000Hz).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Digit Outputs)	+0.3V to −20V
Voltage on Segment and Digit Outputs with respect to V_{SS} pin	+0.3V to −35V
Ambient operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +150°C
Power dissipation	600mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

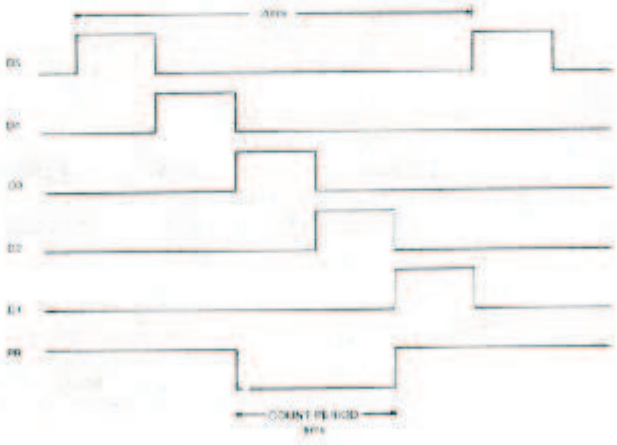
V_{SS} = +5V ±0.5V, V_{DD} = −12V ±1V } or: $V_{SS} - V_{DD}$ = 15.5V to 18.5V
V_B = −28V ±2V
Operating Temperature (T_A) = 0°C to +70°C
Fc = 1.28MHz ±0.01%

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Input logic '0' level	V_{IL}	—	—	+0.8	Volts	
Input logic '1' level	V_{IH}	V_{SS} −1	—	—	Volts	
Input load current (SW, 1.28MHz, OE, MW, CI, CH)	I_{IL}	—	—	0.2	mA	V_{IN} = −V_{SS} Note 1
Input sink current (DMI, SSI, LQ, R)	I_{IH}	—	—	0.2	mA	V_{IN} = +V_{SS} Note 2
Input capacitance	C_{IN}	—	—	10	pF	V_{IN} = OV f = 1MHz
Digit Select Outputs						
Logic '1' On Current		5	—	—	mA	V_{OUT} = (V_{SS} −2)V
Logic '0' Off Current		—	—	10	µA	V_{OUT} = (V_B +1)V
Segment Outputs						
Logic '1' On Current		2	—	—	mA	V_{OUT} = (V_{SS} −2)V
Logic '0' Off Current		—	—	10	µA	V_{OUT} = (V_B +1)V
PR Output						
Logic '0'	V_{OL}	—	—	0.5	Volts	} Load = 2TTL gates (3.2mA), 3.3K
Logic '1'	V_{OH}	V_{SS} −2.2	—	—	Volts	} to V_{DD}, 20pF
Clock input frequency	f_C	—	1.28	1.4	MHz	Note 3
Clock pulse width		350	—	—	ns	logic '0' or '1'
Count input frequency		10	—	500	kHz	
Count input pulse width		600	—	—	ns	logic '0' or '1'
Multiplex rate		—	50	—	kHz	
Power consumption		—	450	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These inputs have resistors of nominally 170K connected to V_{SS}.
2. These inputs have resistors of nominally 170K connected to V_{DD}.
3. For correct frequency readings the clock input frequency must be 1.28 MHz ± 1 in 10^5.

TIMING DIAGRAM



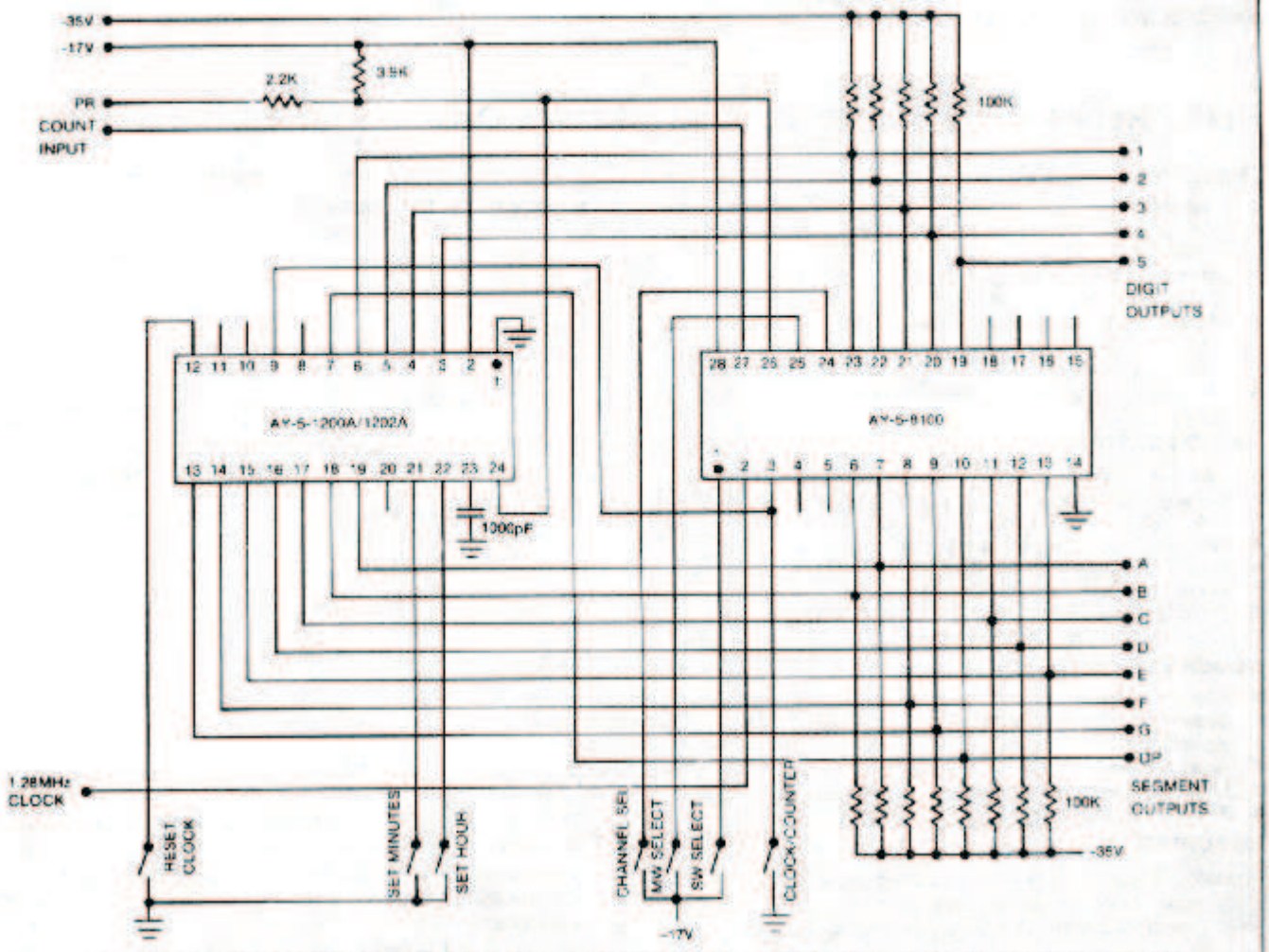


Fig.1 FREQUENCY COUNTER/CLOCK CONNECTION DIAGRAM — DIRECT FLUORESCENT DISPLAY DRIVE.

ENTER-TAINMENT