MOTOROLA

MC13156

Wideband FM IF System

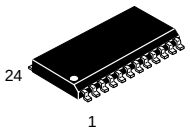
The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved at low cost using Motorola's MOSAIC 1.5™ bipolar process. The MC13156 has an onboard grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multichannel operation. The mixer is useful to 500 MHz and may be used in a balanced–differential, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 2.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 330 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) of –25 dBm (Input Matched)

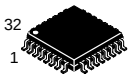
WIDEBAND FM IF SYSTEM FOR DIGITAL AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

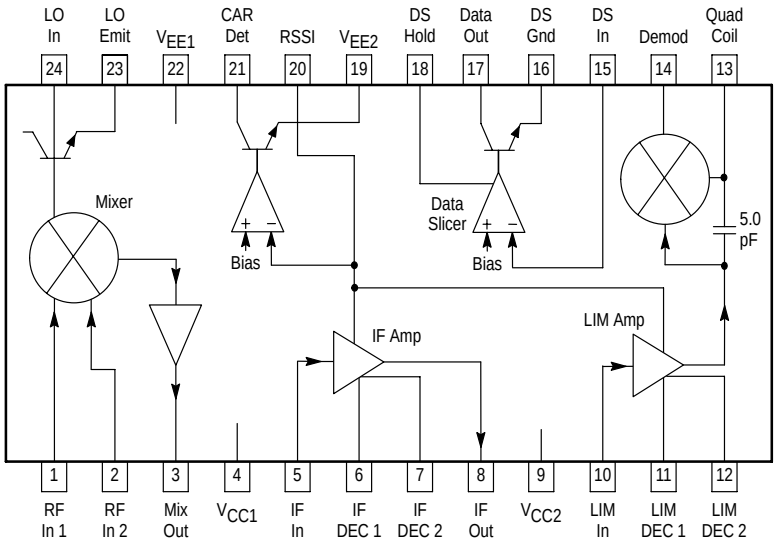


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

FB SUFFIX
PLASTIC QFP PACKAGE
CASE 873



Simplified Block Diagram



NOTE: Pin Numbers shown for SOIC package only. Refer to Pin Assignments Table.

This device contains 197 active transistors.

PIN CONNECTIONS

Function	SO–24L	QFP
RF Input 1	1	31
RF Input 2	2	32
Mixer Output	3	1
V_{CC1}	4	2
IF Amp Input	5	3
IF Amp Decoupling 1	6	4
IF Amp Decoupling 2	7	5
V_{CC} Connect (N/C Internal)	–	6
IF Amp Output	8	7
V_{CC2}	9	8
Limiter IF Input	10	9
Limiter Decoupling 1	11	10
Limiter Decoupling 2	12	11
V_{CC} Connect (N/C Internal)	–	12, 13, 14
Quad Coil	13	15
Demodulator Output	14	16
Data Slicer Input	15	17
V_{CC} Connect (N/C Internal)	–	18
Data Slicer Ground	16	19
Data Slicer Output	17	20
Data Slicer Hold	18	21
V_{EE2}	19	22
RSSI Output/Carrier Detect In	20	23
Carrier Detect Output	21	24
V_{EE1} and Substrate	22	25
LO Emitter	23	26
LO Base	24	27
V_{CC} Connect (N/C Internal)	–	28, 29, 30

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13156DW	T_A = –40 to +85°C	SO–24L
MC13156FB		QFP

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 19, 22	$V_{EE(max)}$	–6.5	Vdc
Junction Temperature	–	$T_{J(max)}$	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" table provides for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage @ T_A = 25°C –40°C ≤ T_A ≤ +85°C	4, 9 16, 19, 22	V_{CC} V_{EE}	0 (Ground) –2.0 to –6.0	Vdc
Input Frequency	1, 2	f_{in}	500	MHz
Ambient Temperature Range	–	T_A	–40 to +85	°C
Input Signal Level	1, 2	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 0, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	19, 22	I_{Total}				mA
V_{EE} = –2.0 Vdc			–	4.8	–	
V_{EE} = –3.0 Vdc			3.0	5.0	8.0	
V_{EE} = –5.0 Vdc			–	5.2	–	
V_{EE} = –6.0 Vdc			–	5.4	–	
Drain Current, I_{22} (See Figure 3)	22	I_{22}				mA
V_{EE} = –2.0 Vdc			–	3.0	–	
V_{EE} = –3.0 Vdc			–	3.1	–	
V_{EE} = –5.0 Vdc			–	3.3	–	
V_{EE} = –6.0 Vdc			–	3.4	–	
Drain Current, I_{19} (See Figure 3)	19	I_{19}				mA
V_{EE} = –2.0 Vdc			–	1.8	–	
V_{EE} = –3.0 Vdc			–	1.9	–	
V_{EE} = –5.0 Vdc			–	1.9	–	
V_{EE} = –6.0 Vdc			–	2.0	–	

DATA SLICER (Input Voltage Referenced to V_{EE} = –3.0 Vdc, no input signal; See Figure 15.)

Input Threshold Voltage (High V_{in})	15	V_{15}	1.0	1.1	1.2	Vdc
Output Current (Low V_{in}) Data Slicer Enabled (No Hold) V_{15} > 1.1 Vdc V_{18} = 0 Vdc	17	I_{17}	–	1.7	–	mA

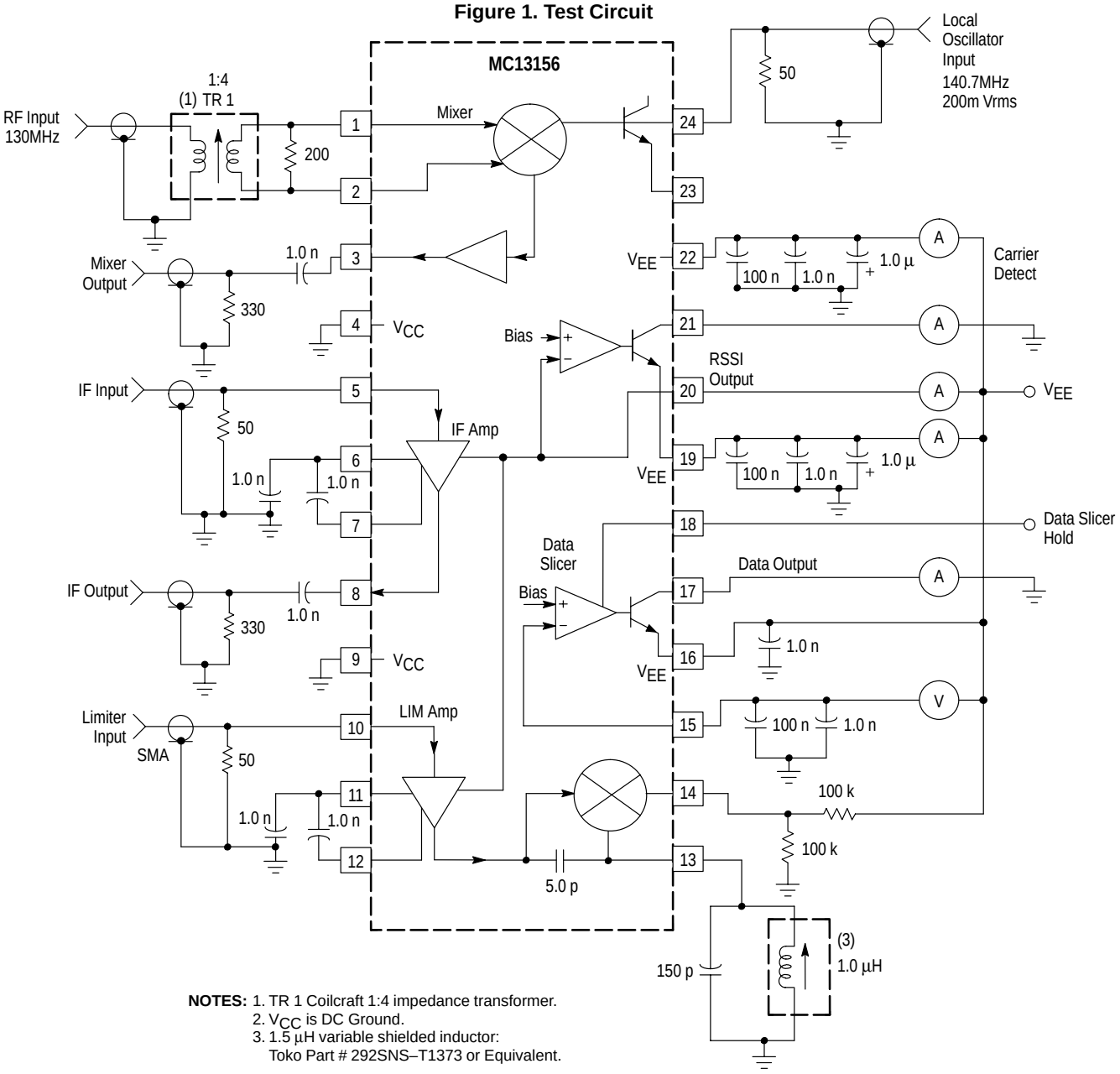
AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figures 17, 25) f_{in} = 144.45 MHz; f_{mod} = 1.0 kHz; f_{dev} = ±75 kHz	1, 14	–	–	–100	–	dBm
MIXER						
Conversion Gain P_{in} = –37 dBm (Figure 4)	1, 3	–	–	22	–	dB
Mixer Input Impedance Single–Ended (Table 1)	1, 2	R_p C_p	– –	1.0 4.0	– –	kΩ pF
Mixer Output Impedance	3	–	–	330	–	Ω
IF AMPLIFIER SECTION						
IF RSSI Slope (Figure 6)	20	–	0.2	0.4	0.6	µA/dB
IF Gain (Figure 5)	5, 8	–	–	39	–	dB
Input Impedance	5	–	–	1.4	–	kΩ
Output Impedance	8	–	–	290	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
LIMITING AMPLIFIER SECTION						
Limiter RSSI Slope (Figure 7)	20	–	0.2	0.4	0.6	µA/dB
Limiter Gain	–	–	–	55	–	dB
Input Impedance	10	–	–	1.4	–	kΩ
CARRIER DETECT						
Output Current – Carrier Detect (High V_{in})	21	–	–	0	–	µA
Output Current – Carrier Detect (Low V_{in})	21	–	–	3.0	–	mA
Input Threshold Voltage – Carrier Detect Input Voltage Referenced to V_{EE} = –3.0 Vdc	20	–	0.9	1.2	1.4	Vdc

Figure 1. Test Circuit



NOTES: 1. TR 1 Coilcraft 1:4 impedance transformer.
2. V_{CC} is DC Ground.
3. 1.5 µH variable shielded inductor:
Toko Part # 292SNS–T1373 or Equivalent.

Figure 2. Total Drain Current versus Supply Voltage and Temperature

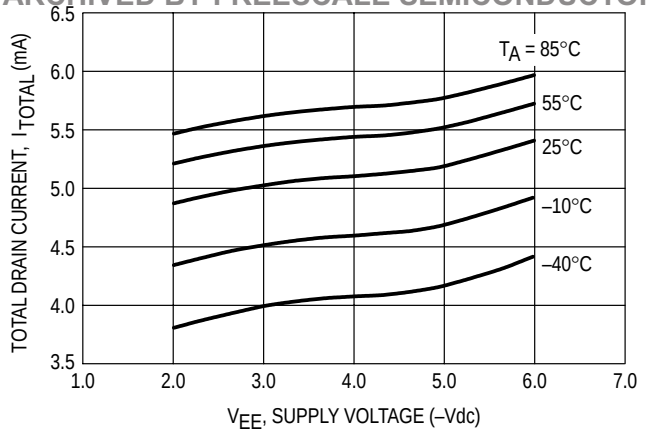


Figure 3. Drain Currents versus Supply Voltage

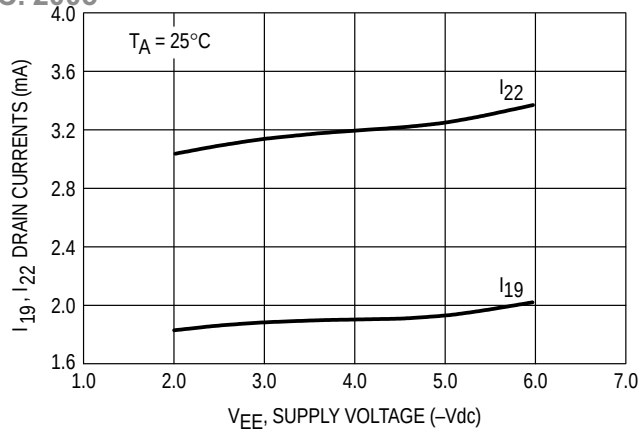


Figure 4. Mixer Gain versus Input Signal Level

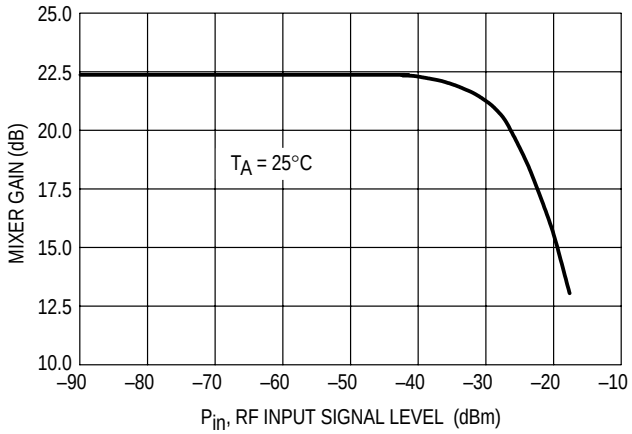


Figure 5. IF Amplifier Gain versus Input Signal Level and Ambient Temperature

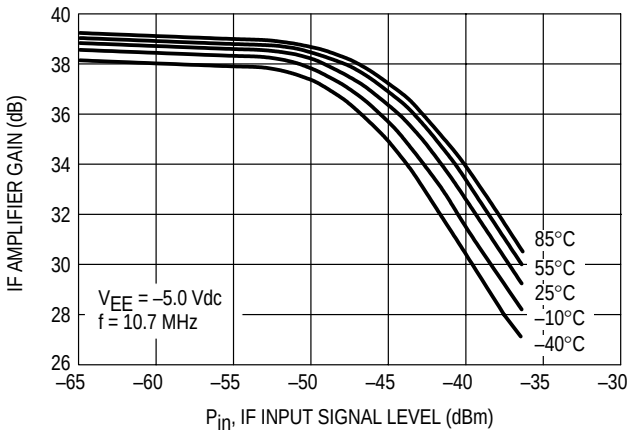


Figure 6. IF Amplifier RSSI Output Current versus Input Signal Level and Ambient Temperature

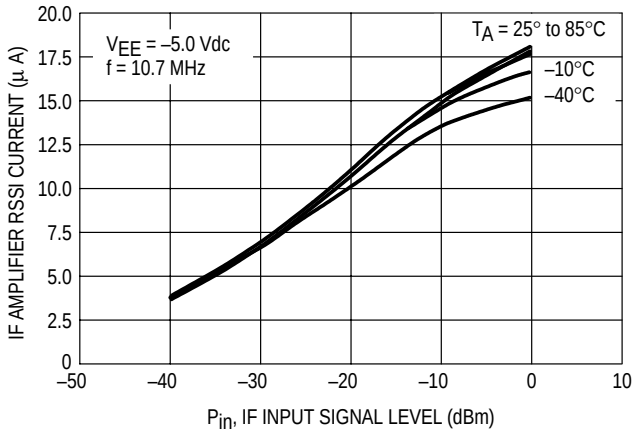
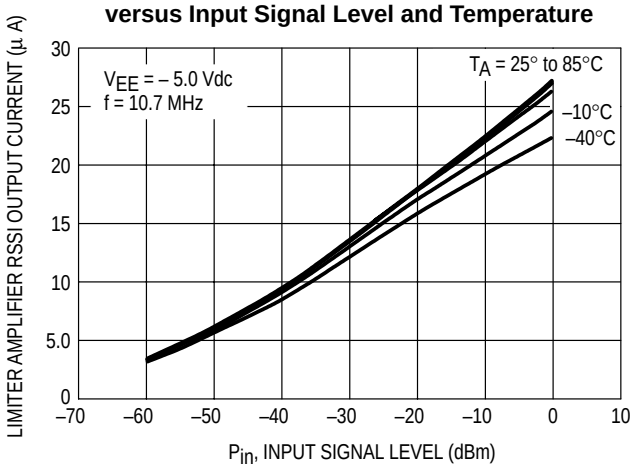


Figure 7. Limiter Amplifier RSSI Output Current versus Input Signal Level and Temperature



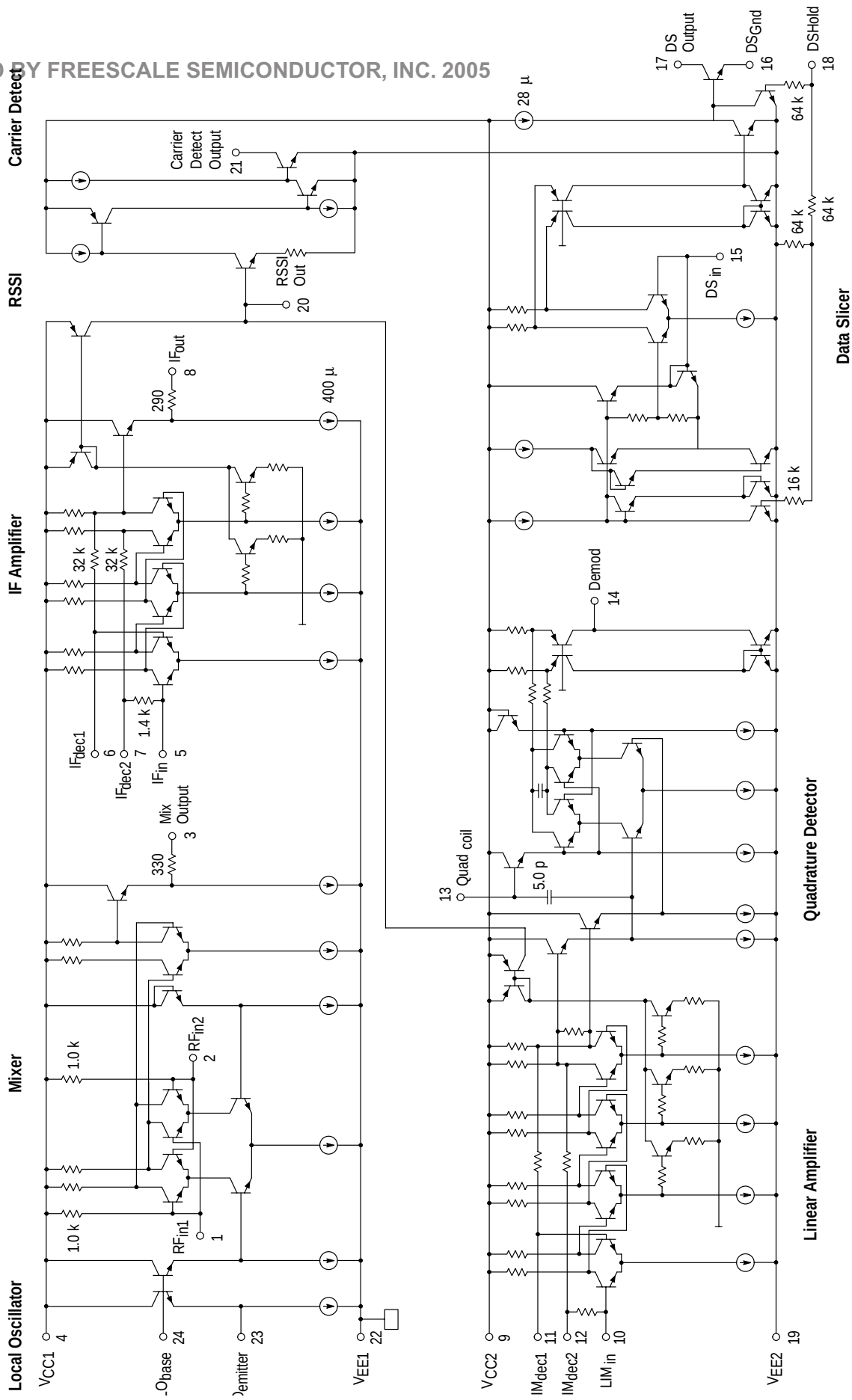


Figure 8. MC13156DW Internal Circuit Schematic

CIRCUIT DESCRIPTION

General

The MC13156 is a low–power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as CT–2 and wideband data links with data rates up to 500 kbaud. It contains a mixer, oscillator, signal strength meter drive, IF amplifier, limiting IF, quadrature detector and a data slicer with a hold function (refer to Figure 8, Simplified Internal Circuit Schematic).

Current Regulation

Temperature compensating voltage independent current regulators are used throughout.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single–ended mode by connecting the other input to the positive supply rail.

Figure 4 shows the mixer gain and saturated output response as a function of input signal drive. The circuit used to measure this is shown in Figure 1. The linear gain of the mixer is approximately 22 dB. Figure 9 shows the mixer gain versus the IF output frequency with the local oscillator of 150 MHz at 100 mVrms LO drive level. The RF frequency is swept. The sensitivity of the IF output of the mixer is shown in Figure 10 for an RF input drive of 10 mVrms at 140 MHz and IF at 10 MHz.

The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 4.0 pF (see Table 1 for details). The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 23 to V_{EE}. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 10).

The oscillator configurations specified above, and two others using an external transistor, are described in the application section:

1) A 133 MHz oscillator multiplier using a 3rd overtone crystal, and
2) A 307.8 to 309.3 MHz manually tuned, varactor controlled local oscillator.

RSSI

The Received Signal Strength Indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 20 sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic or crystal bandpass filters which have an insertion loss of 8.0 dB. The RSSI circuit is designed to provide 70+ dB of dynamic range with temperature compensation (see Figures 6 and 7 which show RSSI responses of the IF and Limiter amplifiers). Variation in the RSSI output current with supply voltage is small (see Figure 11).

Carrier Detect

When the meter current flowing through the meter load resistance reaches 1.2 Vdc above ground, the comparator flips, causing the carrier detect output to go high. Hysteresis can be accomplished by adding a very large resistor for positive feedback between the output and the input of the comparator.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 39 dB at 10.7 MHz. Figure 5 shows the gain and saturated output response of the IF amplifier over temperature, while Figure 12 shows the IF amplifier gain as a function of the IF frequency.

The fixed internal input impedance is 1.4 kΩ. It is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.4 kΩ source and load impedance.

For 10.7 MHz ceramic filter applications, an external 430 Ω resistor must be added in parallel to provide the equivalent load impedance of 330 Ω that is required by the filter; however, no external matching is necessary at the input since the mixer output matches the 330 Ω source impedance of the filter. For 455 kHz applications, an external 1.1 kΩ resistor must be added in series with the mixer output to obtain the required matching impedance of 1.4 kΩ of the filter input resistance. Overall RSSI linearity is dependent on having total midband attenuation of 12 dB (6.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 290 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that four stages are used with the last three contributing to the RSSI. The fixed internal input impedance is 1.4 kΩ. The total gain of the limiting amplifier section is approximately 55 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 9. Mixer Gain versus IF Frequency

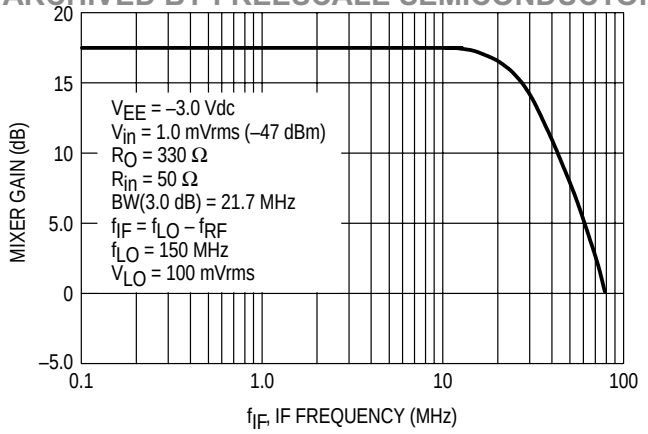


Figure 10. Mixer IF Output Level versus Local Oscillator Input Level

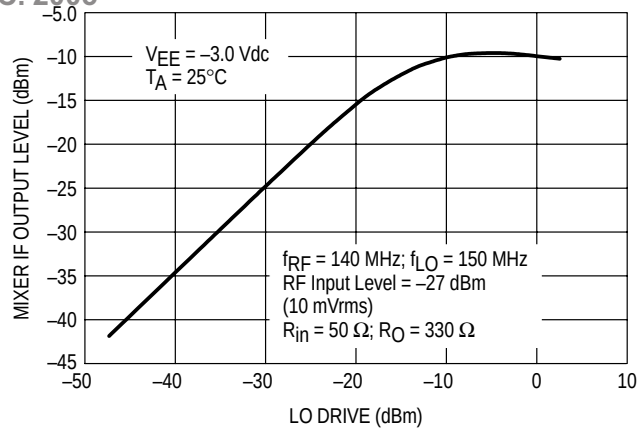


Figure 11. RSSI Output Current versus Supply Voltage and RF Input Signal Level

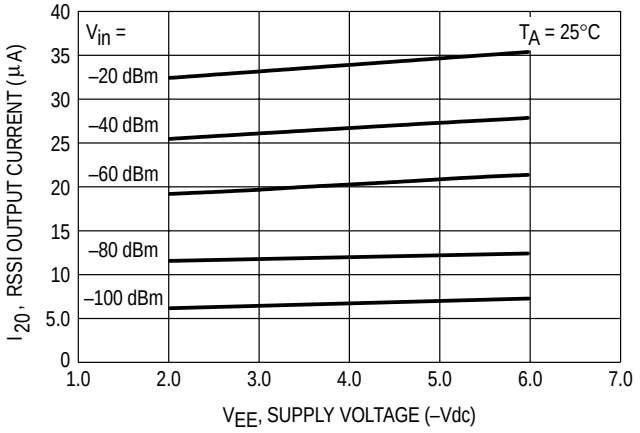


Figure 12. IF Amplifier Gain versus IF Frequency

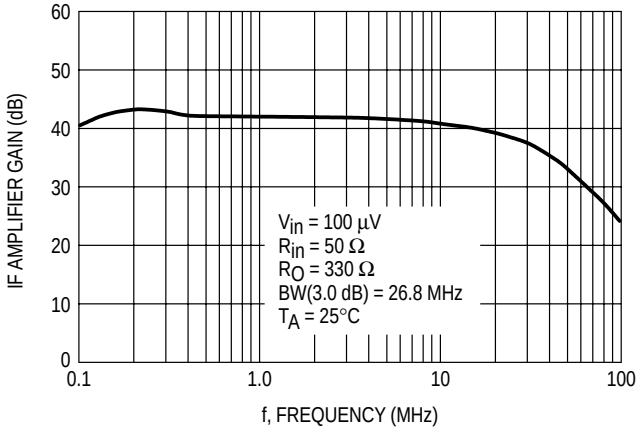
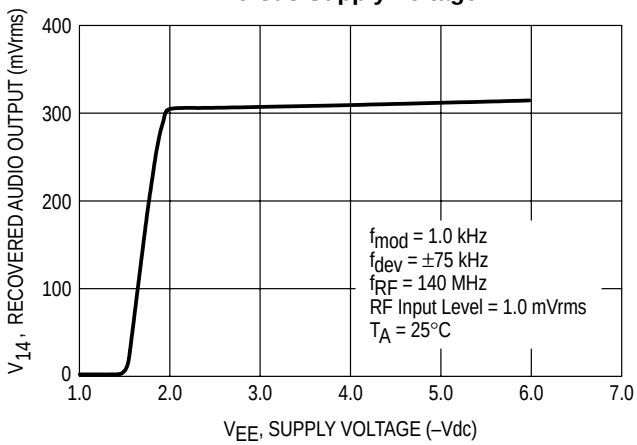


Figure 13. Recovered Audio Output Voltage versus Supply Voltage



Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor to couple the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

The bandwidth of the detector allows for recovery of relatively high data rate modulation. The recovered signal is converted from differential to single ended through a push–pull NPN/PNP output stage. Variation in recovered audio output voltage with supply voltage is very small (see Figure 13). The output drive capability is approximately ±9.0 μA for a frequency deviation of ±75 kHz and 1.0 kHz modulating frequency (see Application Circuit).

Data Slicer

The data slicer input (Pin 15) is self centering around 1.1 V with clamping occurring at $1.1 \pm 0.5\ V_{be}$ Vdc. It is designed to square up the data signal. Figure 14 shows a detailed schematic of the data slicer.

The Voltage Regulator sets up 1.1 Vdc on the base of Q12, the Differential Input Amplifier. There is a potential of 1.0 V_{be} on the base–collector of transistor diode Q11 and 2.0 V_{be} on the base–collector of Q10. This sets up a 1.5 V_{be} (~ 1.1 Vdc) on the node between the 36 kΩ resistors which is connected to the base of Q12. The differential output of the data slicer Q12 and Q13 is converted to a single–ended output by the Driver Circuit. Additional circuitry, not shown in Figure 14, tends to keep the data slicer input centered at 1.1 Vdc as input signal levels vary.

The Input Diode Clamp Circuit provides the clamping at 1.0 V_{be} (0.75 Vdc) and 2.0 V_{be} (1.45 Vdc). Transistor diodes Q7 and Q8 are on, thus, providing a 2.0 V_{be} potential at the base of Q1. Also, the voltage regulator circuit provides a potential of 2.0 Vbe on the base of Q3 and 1.0 V_{be} on the emitter of Q3 and Q2. When the data slicer input (Pin 15) is pulled up, Q1 turns off; Q2 turns on, thereby clamping the input at 2.0 V_{be}. On the other hand, when Pin 15 is pulled down, Q1 turns on; Q2 turns off, thereby clamping the input at 1.0 V_{be}.

The recovered data signal from the quadrature detector is ac coupled to the data slicer via an input coupling capacitor. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in dc level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer. When centered there is no input current allowed, which is to say, that the input looks high in impedance.

Another unique feature of the data slicer is that it responds to various logic levels applied to the Data Slicer Hold Control pin (Pin 18). Figure 15 illustrates how the input and output currents under “no hold” condition relate to the input voltage. Figure 16 shows how the input current and input voltage relate for both the “no hold” and “hold” condition.

The hold control (Pin18) does three separate tasks:

1) With Pin 18 at 1.0 V_{be} or greater, the output is shut off (sets high). Q19 turns on which shunts the base drive from Q20, thereby turning the output off.
2) With Pin 18 at 2.0 V_{be} or greater, internal clamping diodes are open circuited and the comparator input is shut off and effectively open circuited. This is accomplished by turning off the current source to emitters of the input differential amplifier, thus, the input differential amplifier is shut off.
3) When the input is shut off, it allows the input capacitor to hold its charge during transmit to improve recovery at the beginning of the next receive period. When it is turned on, it allows for very fast charging of the input capacitor for quick recovery of new tuning or data average. The above features are very desirable in a TDD digital FM system.

Figure 14. Data Slicer Circuit

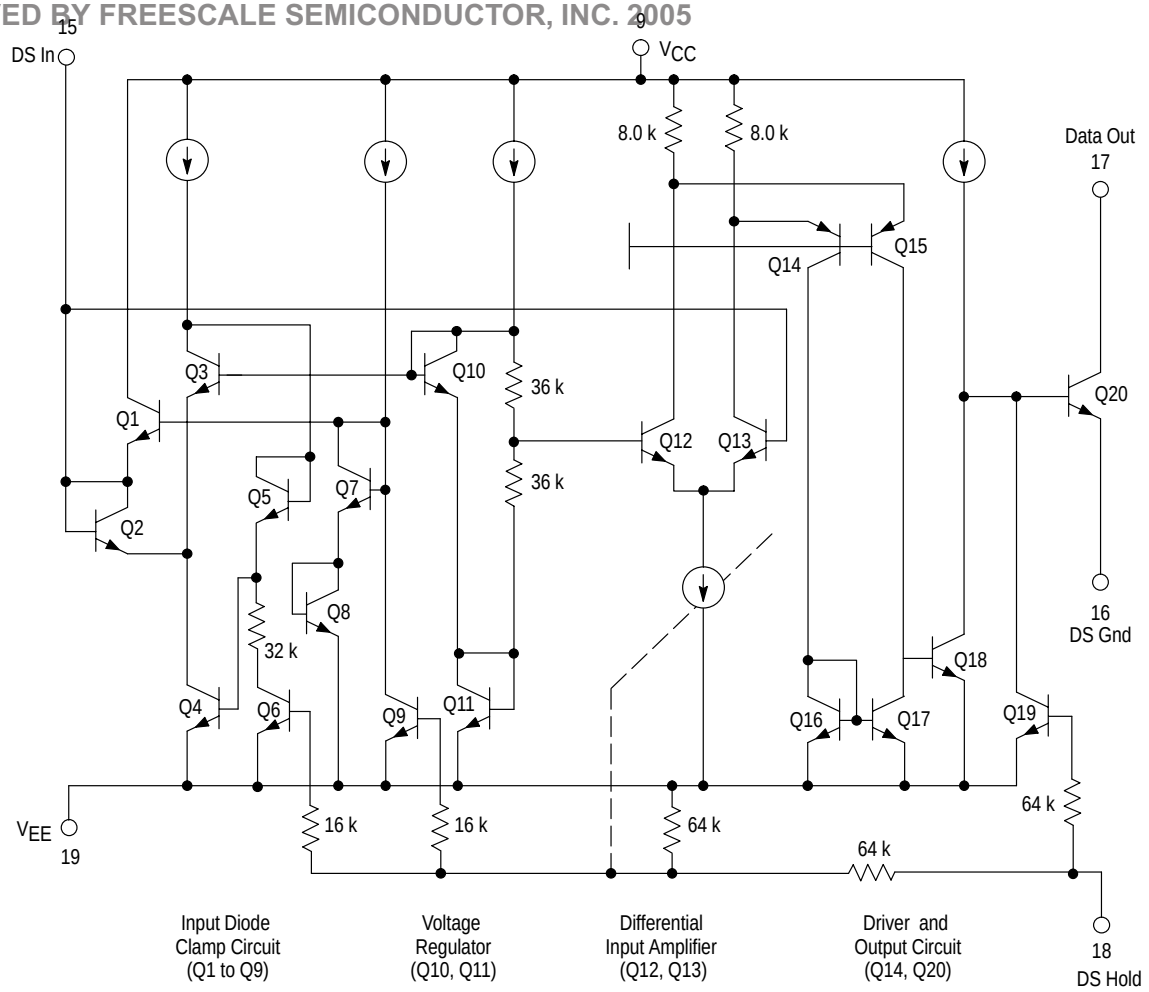


Figure 15. Data Slicer Input/Output Currents versus Input Voltage

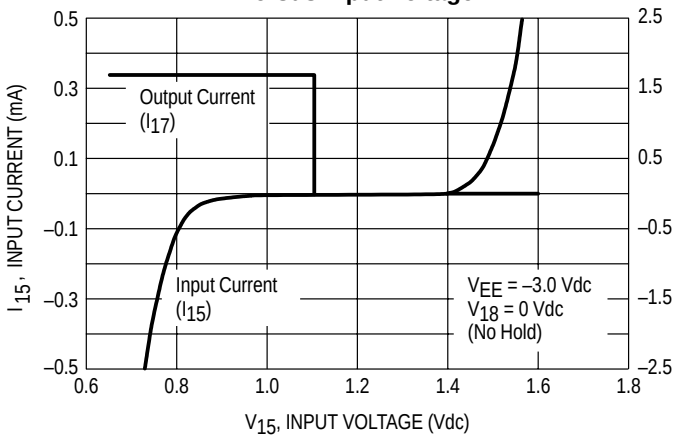


Figure 16. Data Slicer Input Current versus Input Voltage

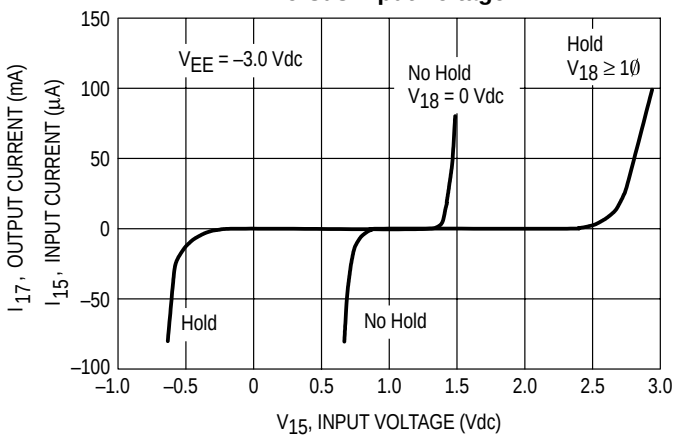
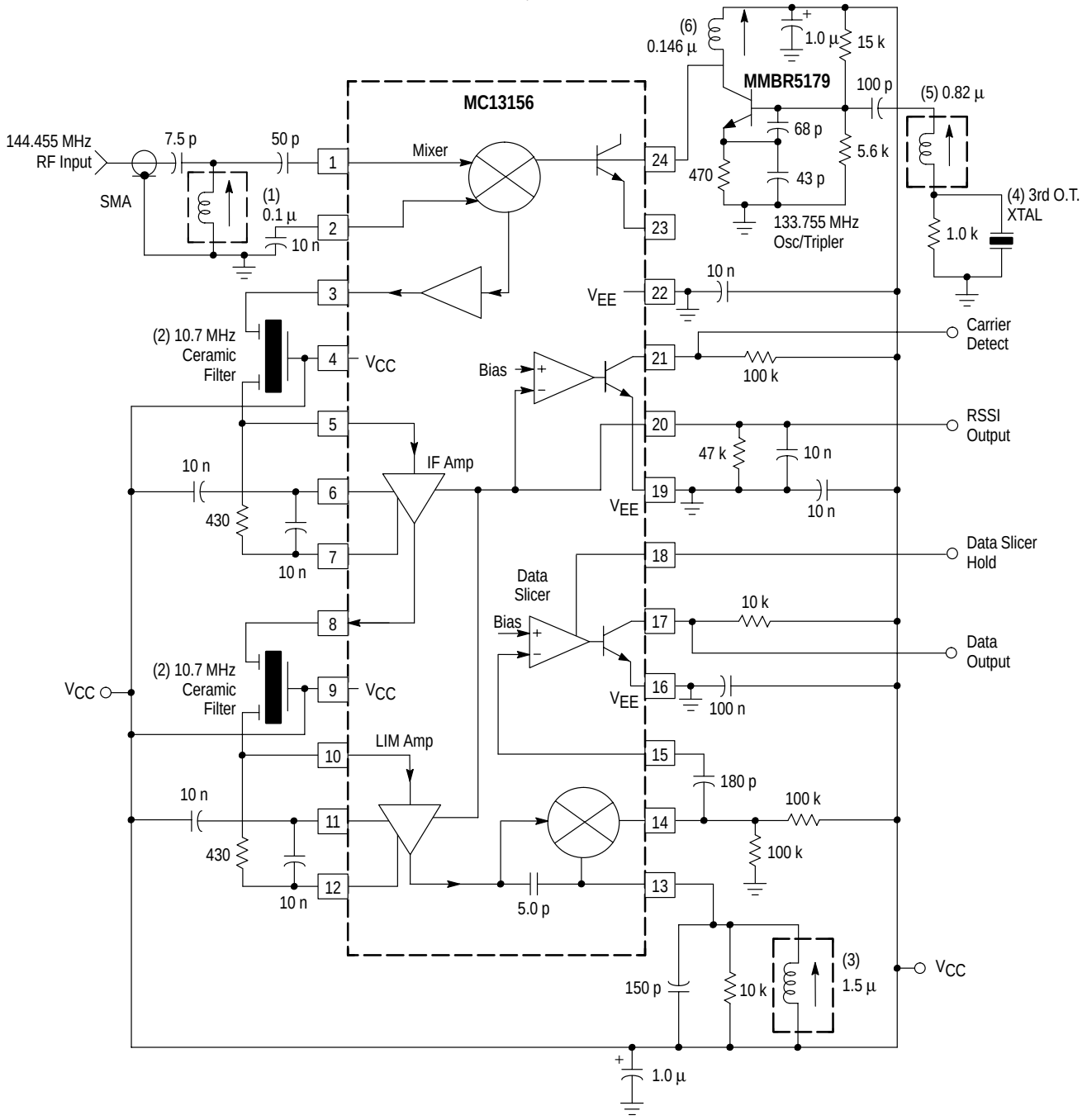


Figure 17. MC13156DW Application Circuit



NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. 10.7 MHz Ceramic Filter: Toko part # SK107M5–A0–10X or Murata Erie part # SFE10.7MHY–A.
3. 1.5 µH Variable Shielded Inductor: Toko part # 292SNS–T1373.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.585 MHz.
5. 0.814 µH Variable Shielded Inductor: Coilcraft part # 143–18J12S.
6. 0.146 µH Variable Inductor: Coilcraft part # 146–04J08.

Figure 18. MC13156DW Circuit Side Component Placement

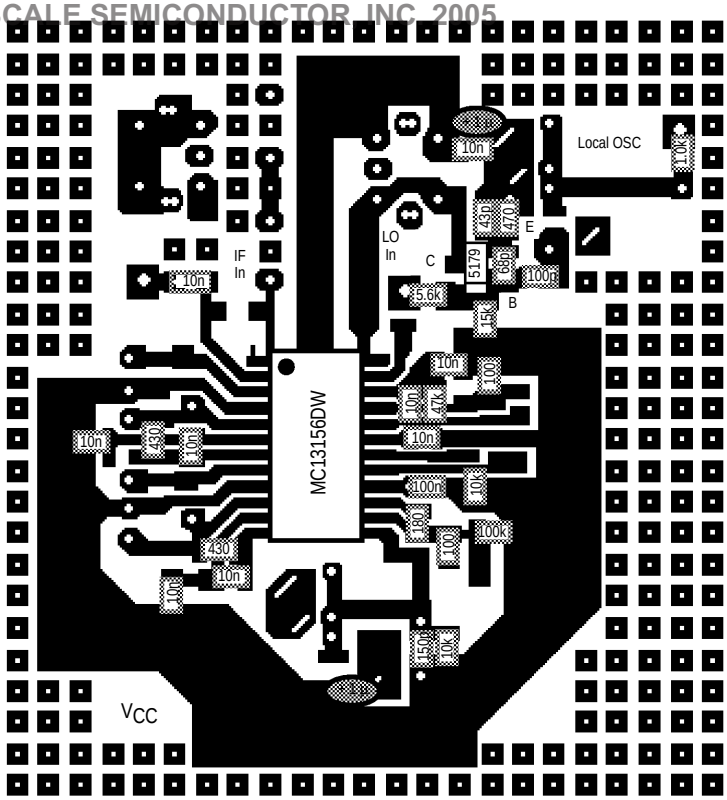
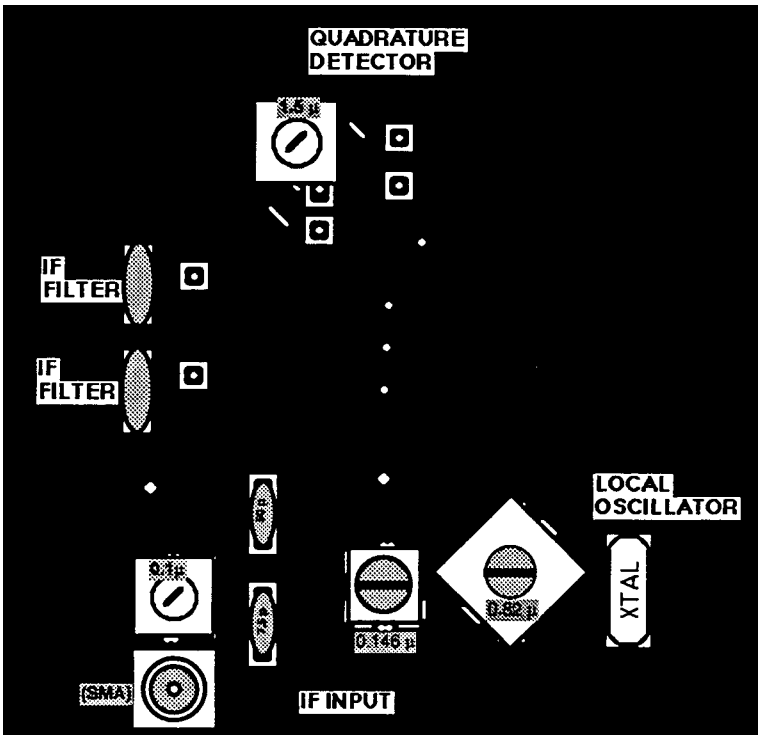


Figure 19. MC13156DW Ground Side Component Placement



APPLICATIONS INFORMATION

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 18 and 19 show the placement for the components specified in the application circuit (Figure 17). The applications circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but equivalent components should give similar results.

Input Matching Networks/Components

The input matching circuit shown in the application circuit schematic is passive high pass network which offers effective image rejection when the local oscillator is below the RF input frequency. Silver mica capacitors are used for their high Q and tight tolerance. The PC board is not dedicated to any particular input matching network topology; space is provided for the designer to breadboard as desired.

Alternate matching networks using 4:1 surface mount transformers or BALUNs provide satisfactory performance. The 12 dB SINAD sensitivity using the above matching networks is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±75 kHz at f_{IN} = 144.45 MHz and f_{OSC} = 133.75 MHz (see Figure 25).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. The SAW filter should be designed to interface with the mixer input impedance of approximately 1.0 kΩ. Table 1 displays the series equivalent single–ended mixer input impedance.

Local Oscillators

VHF Applications – The local oscillator circuit shown in the application schematic utilizes a third overtone crystal and an RF transistor. Selecting a transistor having good phase noise performance is important; a mandatory criteria is for the device to have good linearity of beta over several decades of collector current. In other words, if the low current beta is suppressed, it will not offer good 1/f noise performance. A third overtone series resonant crystal having at least 25 ppm tolerance over the operating temperature is recommended. The local oscillator is an impedance inversion third overtone Colpitts network and harmonic generator. In this circuit a 560 to 1.0 kΩ resistor shunts the crystal to ensure that it operates in its overtone mode; thus, a blocking capacitor is needed to eliminate the dc path to ground. The resulting parallel LC network should “free–run” near the crystal frequency if a short to ground is placed across the crystal. To provide sufficient output loading at the collector, a high Q variable inductor is used that is tuned to self resonate at the 3rd harmonic of the overtone crystal frequency.

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. Figure 20 shows a 5th overtone oscillator at 93.3 MHz and Figure 21 shows a 7th overtone oscillator at 148.3 MHz. Both circuits use a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have good tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and startup of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high, the performance of the oscillator may be impacted by lower gain margins.

Table 1. Mixer Input Impedance Data
(Single–ended configuration, V_{CC} = 3.0 Vdc, local oscillator drive = 100 mVrms)

Frequency (MHz)	Series Equivalent Complex Impedance (R + jX) (Ω)	Parallel Resistance Rp (Ω)	Parallel Capacitance Cp (pF)
90	190 – j380	950	4.7
100	160 – j360	970	4.4
110	130 – j340	1020	4.2
120	110 – j320	1040	4.2
130	97 – j300	1030	4.0
140	82 – j280	1040	4.0
150	71 – j270	1100	4.0
160	59 – j260	1200	3.9
170	52 – j240	1160	3.9
180	44 – j230	1250	3.8
190	38 – j220	1300	3.8

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 24) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_O, provides a feedback path that is low enough in reactance at frequencies of 5th overtone or higher to cause trouble. C_O has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor (L_O) is placed in parallel with the crystal. L_O is chosen to resonant with the crystal parallel capacitance (C_O) at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

UHF Application

Figure 22 shows a 318.5 to 320 MHz receiver which drives the mixer with an external varactor controlled (307.8 to 309.3 MHz) LC oscillator using an MPS901 (RF low power transistor in a TO–92 plastic package; also MMBR901 is available in a SOT–23 surface mount package). With the 50 kΩ 10 turn potentiometer this oscillator is tunable over a range of approximately 1.5 MHz. The MMBV909L is a low voltage varactor suitable for UHF applications; it is a dual back–to–back varactor in a SOT–23 package. The input matching network uses a 1:4 impedance matching transformer (Recommended sources are Mini–Circuits and Coilcraft).

Using the same IF ceramic filters and quadrature detector circuit as specified in the applications circuit in Figure 17, the 12 dB SINAD performance is –95 dBm for a f_{mod} = 1.0 kHz sinusoidal waveform and f_{dev} ±40 kHz.

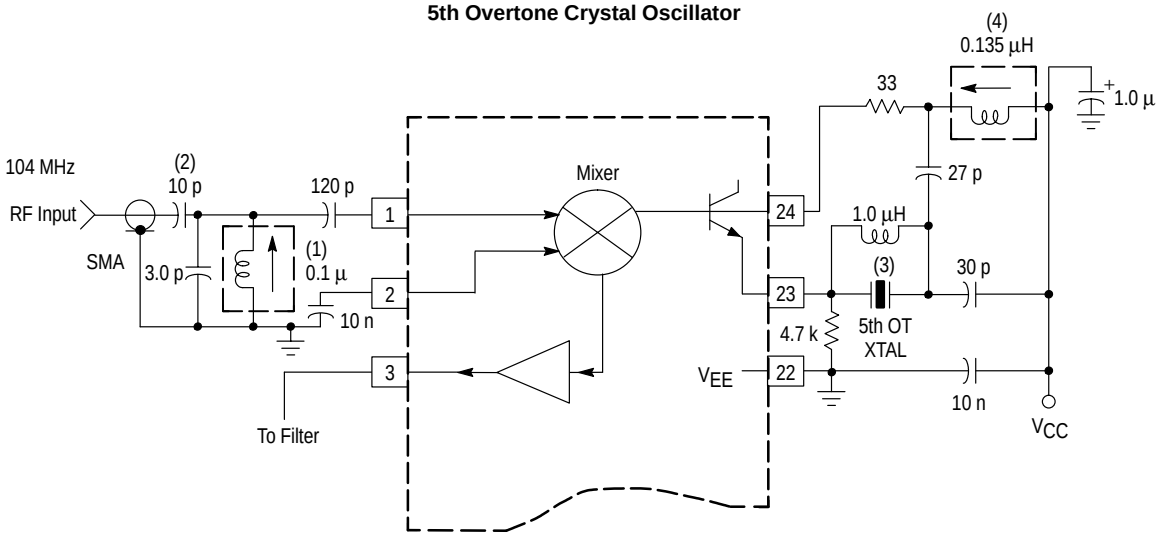
This circuit is breadboarded using the evaluation PC board shown in Figures 32 and 33. The RF ground is V_{CC} and path lengths are minimized. High quality surface mount components were used except where specified. The absolute values of the components used will vary with layout placement and component parasitics.

RSSI Response

Figure 26 shows the full RSSI response in the application circuit. The 10.7 MHz, 110 kHz wide bandpass ceramic filters (recommended sources are TOKO part # SK107M5–AO–10X or Murata Erie SFE10.7MHY–A) provide the correct bandpass insertion loss to linearize the curve between the limiter and IF portions of RSSI. Figure 25 shows that limiting occurs at an input of –100 dBm. As shown in Figure 26, the RSSI output linear from –100 dBm to –30 dBm.

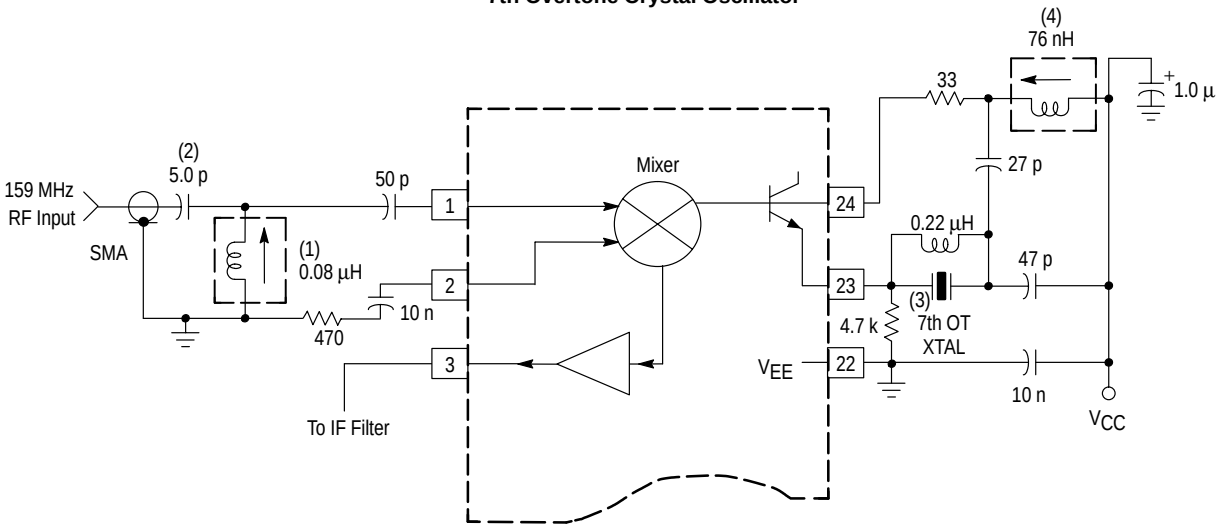
The RSSI rise and fall times for various RF input signal levels and R20 values are measured at Pin 20 without 10 nF filter capacitor. A 10 kHz square wave pulses the RF input signal on and off. Figure 27 shows that the rise and fall times are short enough to recover greater than 10 kHz ASK data; with a wider IF bandpass filters data rates up to 50 kHz may be achieved. The circuit used is the application circuit in Figure 17 with no RSSI output filter capacitor.

Figure 20. MC13156DW Application Circuit
f_{RF} = 104 MHz; f_{LO} = 93.30 MHz
5th Overtone Crystal Oscillator



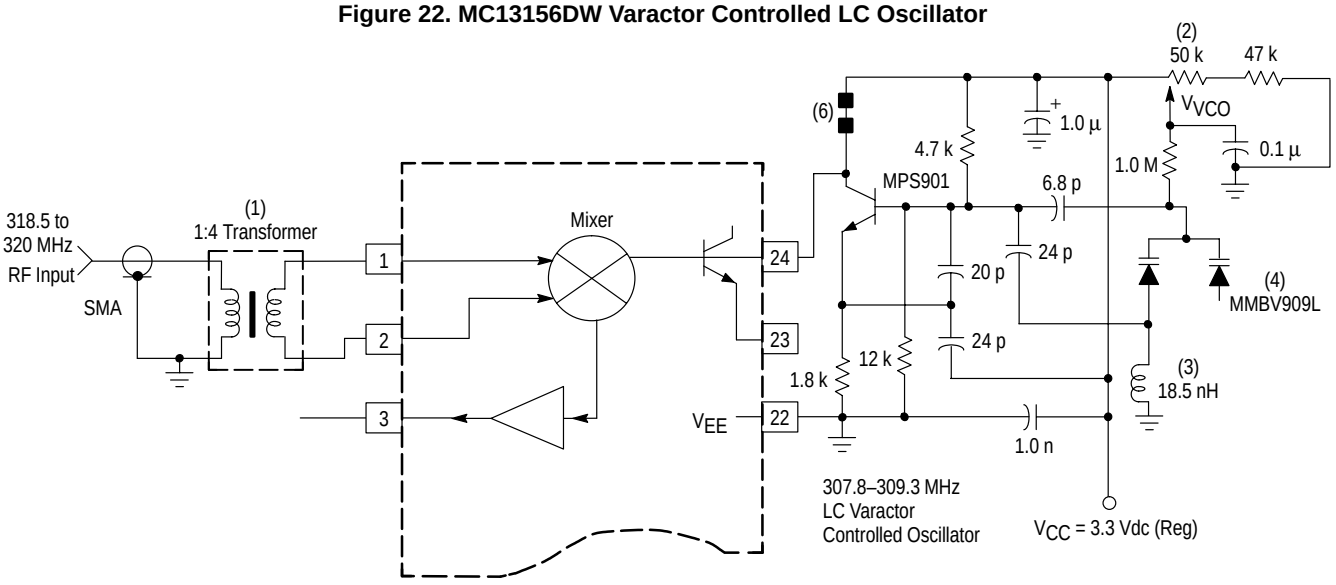
NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. Capacitors are Silver Mica.
3. 5th Overtone, Series Resonant, 25 PPM Crystal at 93.300 MHz.
4. 0.135 µH Variable Shielded Inductor: Coilcraft part # 146–05J08S or equivalent.

Figure 21. MC13156DW Application Circuit
f_{RF} = 159 MHz; f_{LO} = 148.30 MHz
7th Overtone Crystal Oscillator



NOTES: 1. 0.08 µH Variable Shielded Inductor: Toko part # 292SNS–T1365Z or equivalent.
2. Capacitors are Silver Mica.
3. 7th Overtone, Series Resonant, 25 PPM Crystal at 148.300 MHz.
4. 76 nH Variable Shielded Inductor: Coilcraft part # 150–03J08S or equivalent.

Figure 22. MC13156DW Varactor Controlled LC Oscillator



NOTES: 1. 1:4 Impedance Transformer: Mini–Circuits.
2. 50 k Potentiometer, 10 turns.
3. Spring Coil; Coilcraft A05T.
4. Dual Varactor in SOT–23 Package.
5. All other components are surface mount components.
6. Ferrite beads through loop of 24 AWG wire.

45 MHz Narrowband Receiver

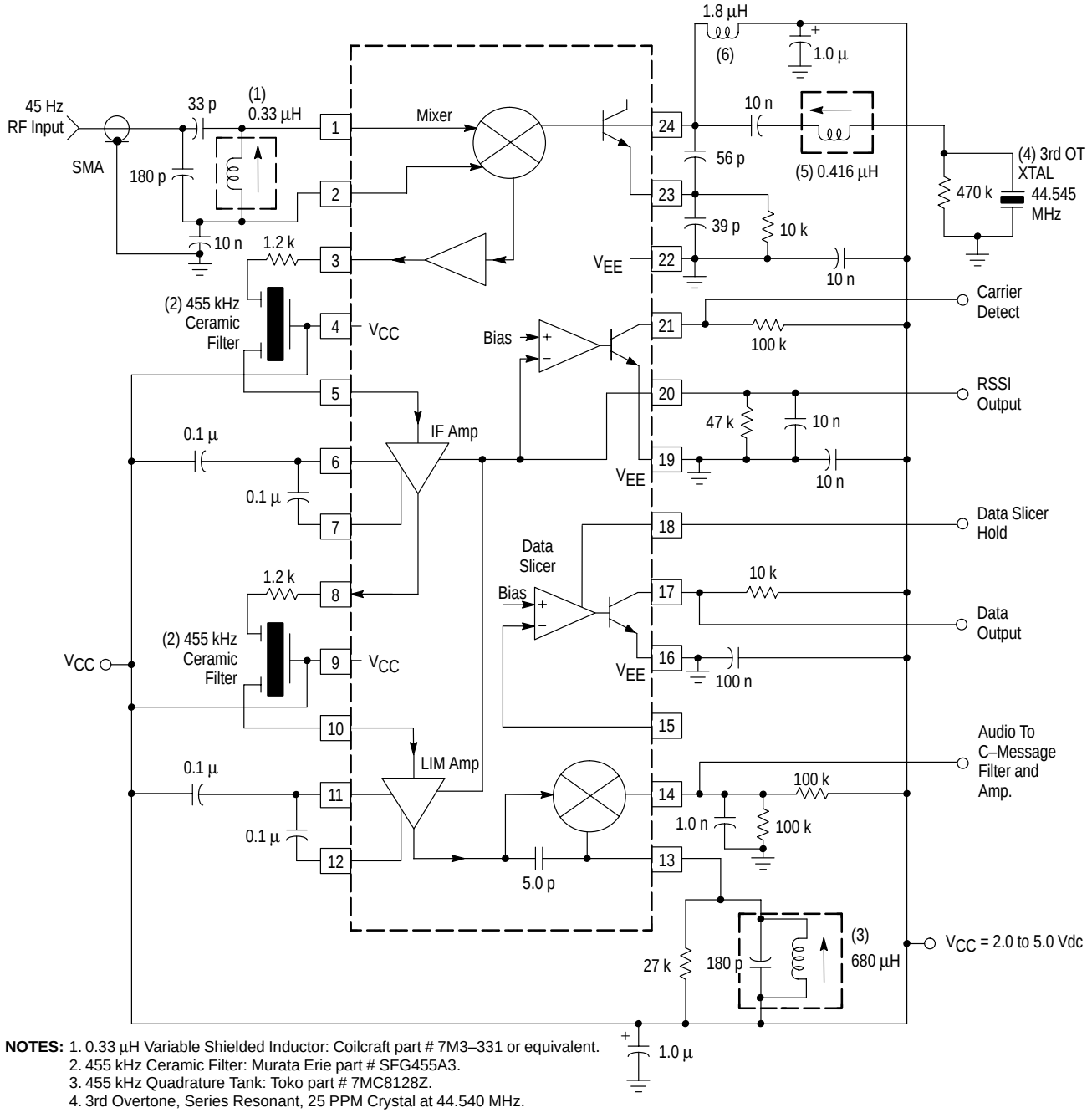
The above application examples utilize a 10.7 MHz IF. In this section a narrowband receiver with a 455 kHz IF will be described. Figure 23 shows a full schematic of a 45 MHz receiver that uses a 3rd overtone crystal with the on–chip oscillator transistor. The oscillator configuration is similar to the one used in Figure 17; it is called an impedance inversion Colpitts. A 44.545 MHz 3rd overtone, series resonant crystal is used to achieve an IF frequency at 455 kHz. The ceramic IF filters selected are Murata Erie part # SFG455A3. 1.2 kΩ chip resistors are used in series with the filters to achieve the terminating resistance of 1.4 kΩ to the filter. The IF decoupling is very important; 0.1 μF chip capacitors are used at Pins 6, 7, 11 and 12. The quadrature detector tank circuit uses a 455 kHz quadrature tank from Toko.

The 12 dB SINAD performance is –109 dBm for a f_{mod} = 1.0 kHz and a f_{dev} = ±4.0 kHz. The RSSI dynamic range is approximately 80 dB of linear range (see Figure 24).

Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 28. This information helps determine the network topology and gain blocks required ahead of the MC13156 to achieve the desired sensitivity and dynamic range of the receiver system. In the application circuit the input third order intercept (IP3) performance of the system is approximately –25 dBm (see Figure 29).

Figure 23. MC13156DW Application Circuit at 45 MHz



NOTES: 1. 0.33 μH Variable Shielded Inductor: Coilcraft part # 7M3–331 or equivalent.
2. 455 kHz Ceramic Filter: Murata Erie part # SFG455A3.
3. 455 kHz Quadrature Tank: Toko part # 7MC8128Z.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.540 MHz.
5. 0.416 μH Variable Shielded Inductor: Coilcraft part # 143–10J12S.
6. 1.8 μH Molded Inductor.

Figure 24. RSSI Output Voltage versus Input Signal Level

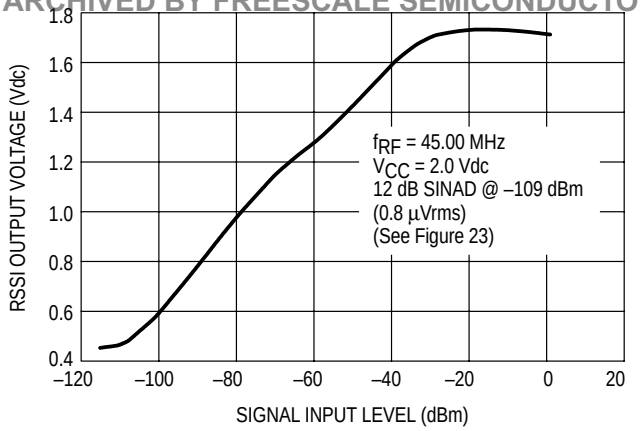


Figure 25. S + N/N versus RF Input Signal Level

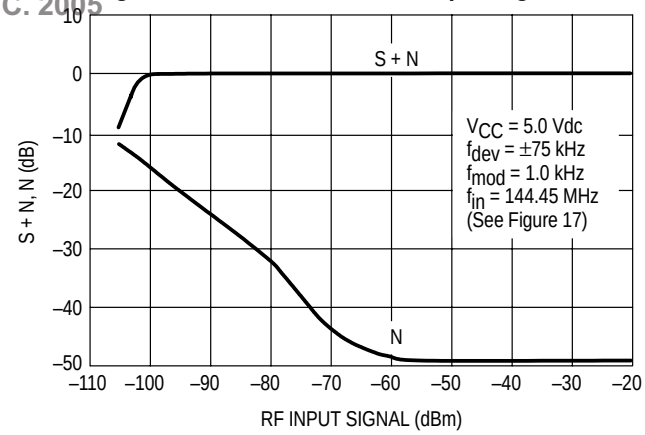


Figure 26. RSSI Output Voltage versus Input Signal Level

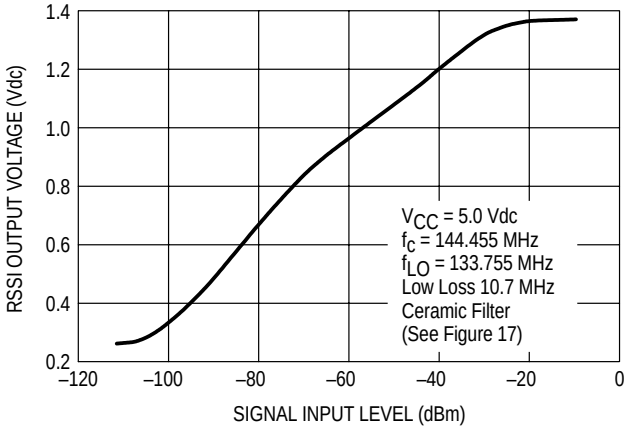


Figure 27. RSSI Output Rise and Fall Times versus RF Input Signal Level

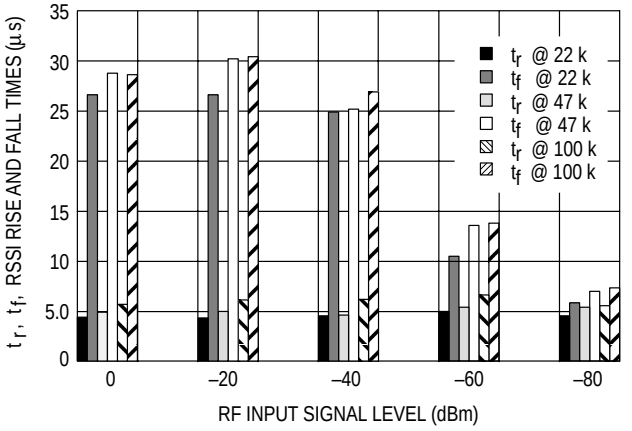


Figure 28. Signal Levels versus RF Input Signal Level

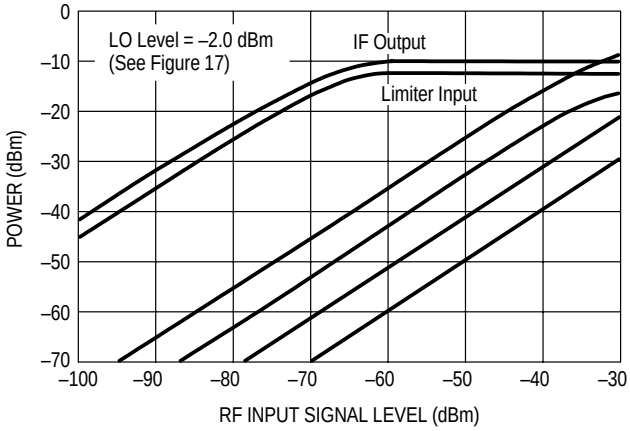
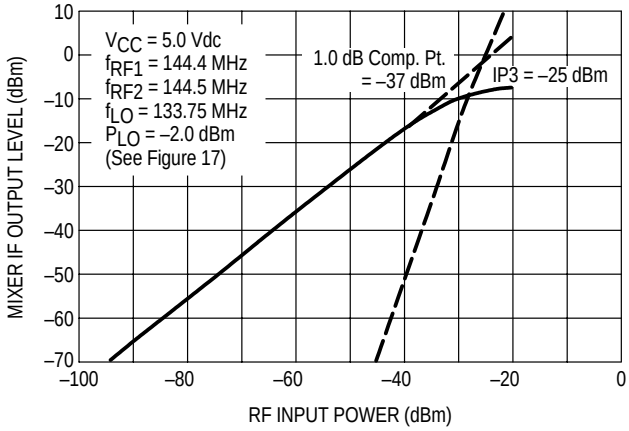


Figure 29. 1.0 dB Compression Pt. and Input Third Order Intercept Pt. versus Input Power



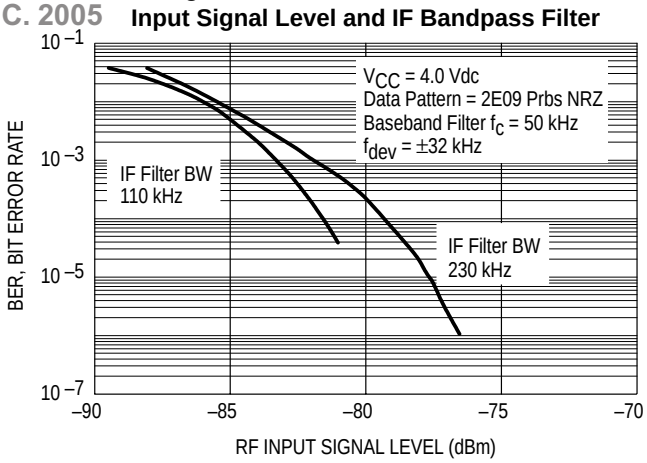
Description

The test setup shown in Figure 31 is configured so that the function generator supplies a 100 kHz clock source to the bit error rate tester. This device generates and receives a repeating data pattern and drives a 5 pole baseband data filter. The filter effectively reduces harmonic content of the baseband data which is used to modulate the RF generator which is running at 144.45 MHz. Following processing of the signal by the receiver (MC13156), the recovered baseband sinewave (data) is AC coupled to the data slicer. The data slicer is essentially an auto–threshold comparator which tracks the zero crossing of the incoming sinewave and provides logic level data at its ouput. Data errors associated with the recovered data are collected by the bit error rate receiver and displayed.

Bit error rate versus RF signal input level and IF filter bandwidth are shown in Figure 30. The bit error rate data was taken under the following test conditions:

- Data rate = 100 kbps
- Filter cutoff frequency set to 39% of the data rate or 39 kHz.
- Filter type is a 5 pole equal–ripple with 0.5° phase error.
- V_{CC} = 4.0 Vdc
- Frequency deviation = ±32 kHz.

Figure 30. Bit Error Rate versus RF Input Signal Level and IF Bandpass Filter



Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 32 and 33). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates.

Figure 31. Bit Error Rate Test Setup

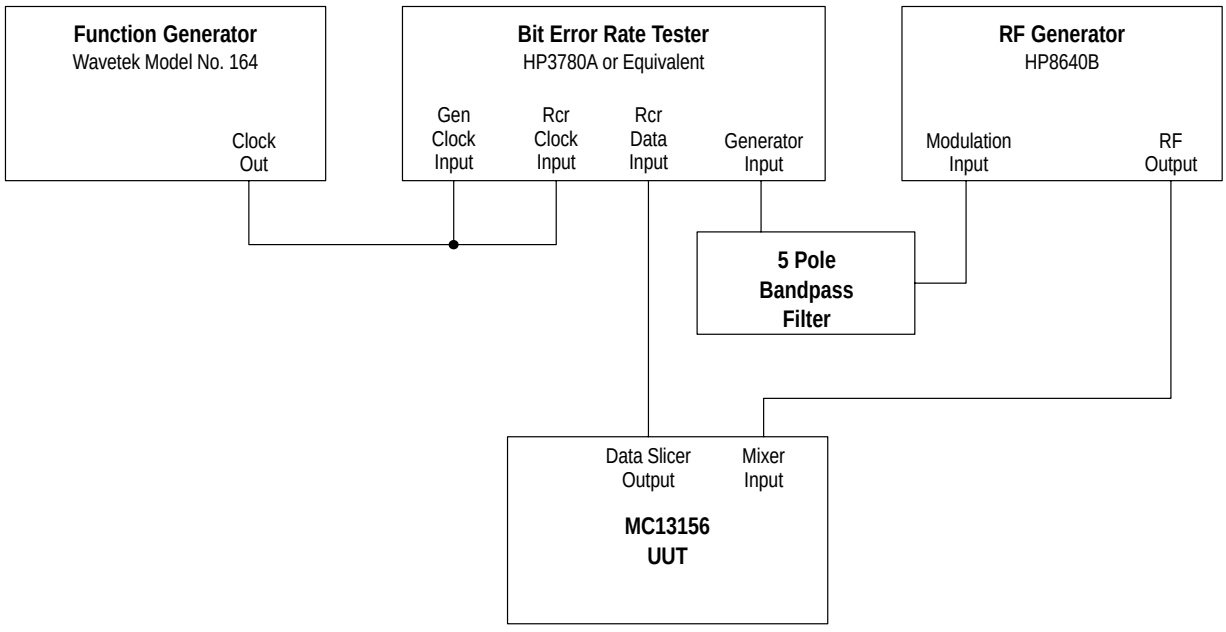


Figure 32. Circuit Side View

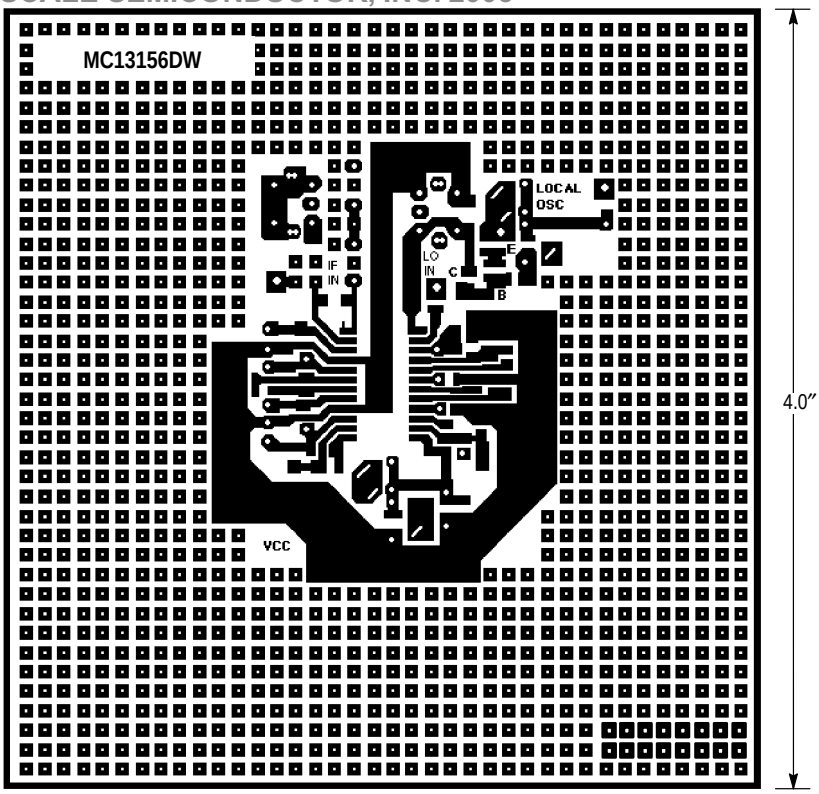
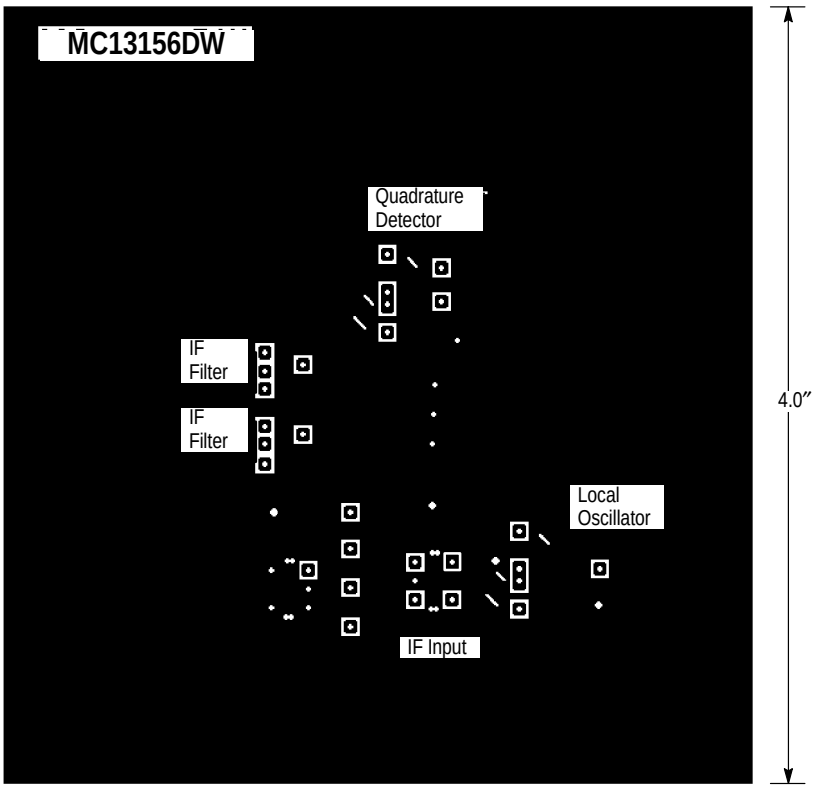
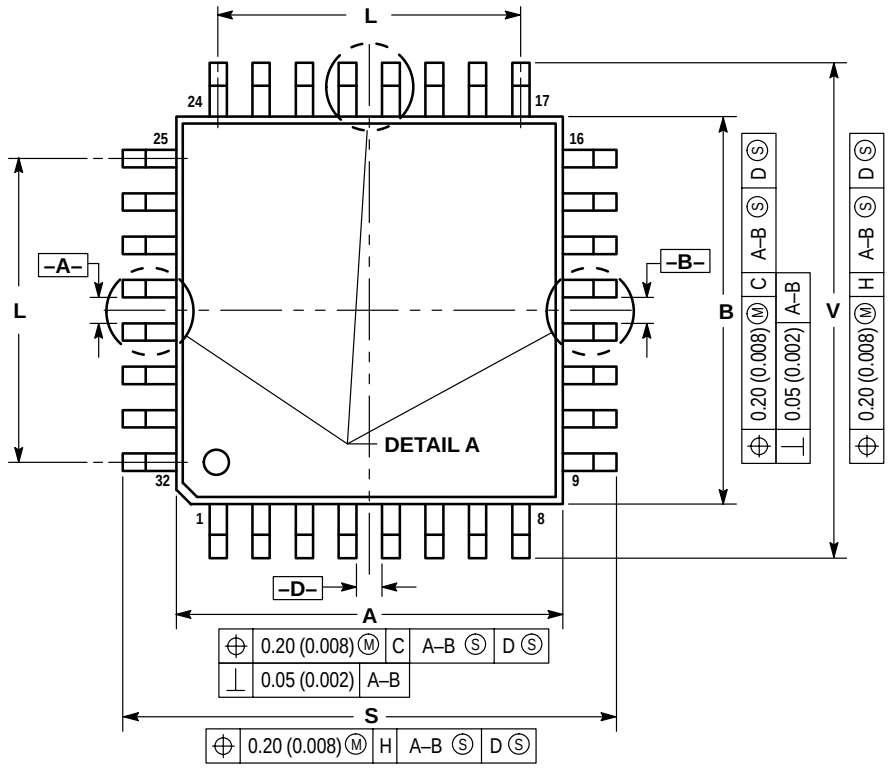


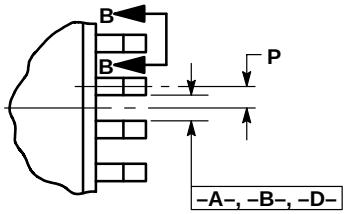
Figure 33. Ground Side View



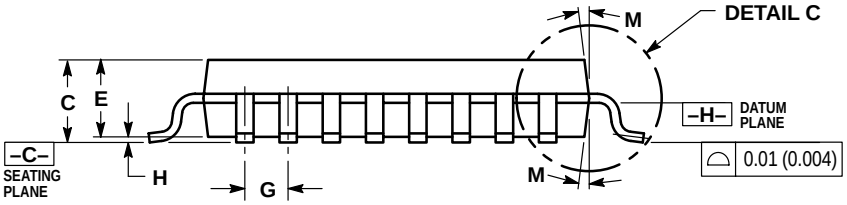
OUTLINE DIMENSIONS

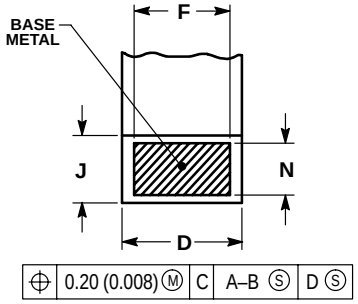
FB SUFFIX
PLASTIC QFP PACKAGE
CASE 873–01
ISSUE A



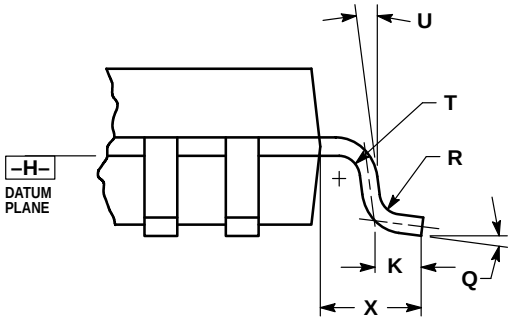


DETAIL A





SECTION B–B
VIEW ROTATED 90 ° CLOCKWISE



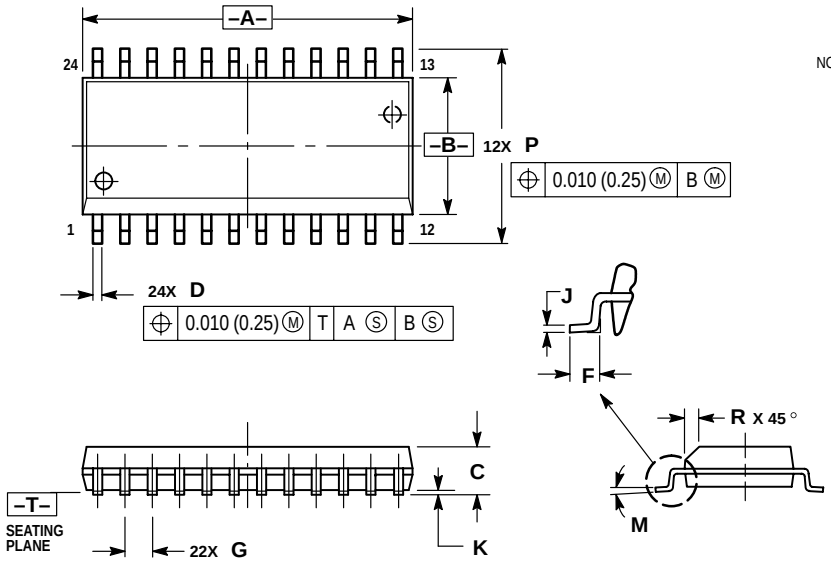
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6 °	8 °	6 °	8 °
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5 °	10°	5 °	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5 °	11°	5 °	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC PACKAGE
CASE 751E–04
(SO–24L)
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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